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(54) Enhanced L1/L2 code channel for global positioning system receivers.

(57) An enhanced P-code channel (60) for use in a GPS receiver (10) to simultaneously track L1 and L2 comprises a P-code clock generator (62) for generating two code clocks. The first code clock associates with L1 and the second associates with L2. The code clocks have the same frequency but different phases from one another. Circuitry (64) and (66) generate and store a plurality of P-code chips. A first circuit (68, 70) selects and updates P-code chips from the stored P-code chips that are in phase with the L1 code clock. A second circuit (72 and 74) selects and updates P-code chips from the P-code chips and phased with the L2 code clock.

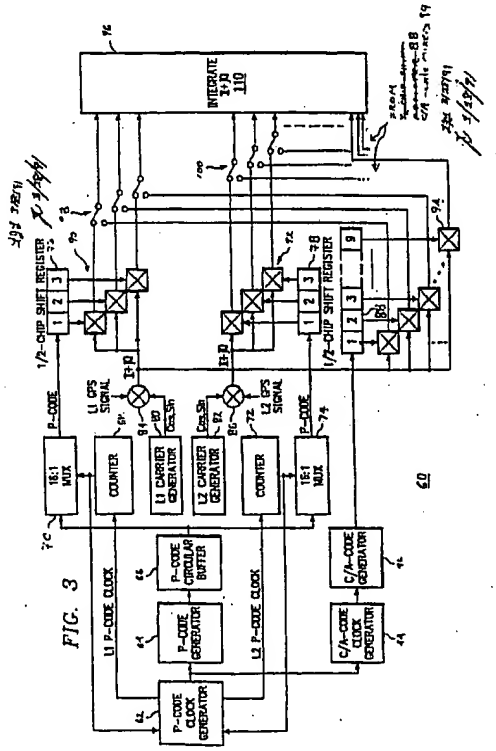

FIG. 3

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SUMMARY OF THE INVENTION

Accordingly, the present invention provides inventive subject matter which overcomes the problems associated with ionospheric delay in Global Positioning System (GPS) receivers. In particular, the present invention provides a single enhanced precision code (P-code) channel for use in a GPS receiver that can simultaneously track L1 and L2 from a single satellite.

The enhanced P-code channel includes a single P-code clock generator for generating two code clock signals (L1 and L2) with the same frequency but a different phase. A P-code generator uses one of the P-code clocks to generate a continuous P-code data stream. Circuitry then stores a plurality of the most recently generated P-code chips. A counter and multiplexer circuit is then used to maintain a constant P-code stream (which may be delayed from the output of the P-code generator) by using one of the P-code clocks. In addition, carrier generation and mixing circuitry, code delay shift registers and mixing circuitry, and multiple pre-detection accumulators exist to allow for the simultaneous tracking of L1 and L2 signals.

A technical advantage of the present system is that, by enhancing a single P-code channel, it is possible to obtain the benefit of independent L1 and L2 tracking loops within a GPS system without the penalty of having two independent hardware channels for this purpose.

Another technical advantage of the present invention is that it is possible to gain the benefit of tracking L2 in addition to L1 to reduce error introduced by ionospheric delay, without the additional processor throughput requirements of tracking L2 independently.

Yet another technical advantage of the present invention is that it permits making continual L1 and L2 calculations without the need for additional computing and support equipment.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be acquired by referring to the detailed description and claims when considered in connection with the accompanying drawings in which like reference numerals indicate like features wherein:

FIGURE 1 is a block diagram of a GPS receiver that may use the enhanced L1/L2 channel of the present invention;

FIGURE 2 is a block diagram of a typical C/A- and P-code channel for use in a GPS receiver for receiving L1 and L2.

FIGURE 3 is a block diagram of a preferred embodiment of the enhanced P-code channel for tracking L1 and L2 for GPS applications;

FIGURE 4 is a block diagram representing the P-code clock generator according to a preferred embodiment of the present invention;

FIGURE 5 provides a comparison chart between a typical and enhanced P-code channel for tracking L1 and L2 of the present invention.

Figure 6 shows a block diagram of PCOAC 1010. Unused functions can be turned off allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Figure 7 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC 10: Base Band Module 1130 generates several global clocks for system synchronization;

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present invention is best understood by referring to the FIGUREs wherein like numbers are used for like corresponding parts of the various components.

To understand the present invention, it is best to understand the environment of the preferred embodiment. For this purpose, FIGURE 1 provides a simple block diagram of a Global Positioning System (GPS) navigation receiver. The system of FIGURE 1 is described in more detail in U.S. Patent Application Serial No. (TI Docket No TI-15358) to John P. Volpi et al and assigned to Texas Instruments Incorporated entitled "System and Method for Digital Navigation Satellite Receiver" and U.S. Patent Application Serial No. (TI Docket No. TI-15357) to Leonard LaPadula III, et al, also assigned to Texas Instruments Incorporated, entitled "Method and System for Multi-Channel and Search Global Position System Signal Processor" both filed on February 28, 1991. U.S. Patent Application Serial Nos. and are hereby expressly incorporated by reference in their entirety.

FIGURE 1 is a simple block diagram of the whole receiver. A single RF path amplifies and down-converts the L1 or L2 signal to an intermediate frequency (IF). The receiver performs analog-to-digital conversion before any GPS signal processing takes place. After the signal is digitized, the signal is processed in three signal processing chips (SPC). The SPCs perform all the GPS hardware signal processing.

Referring more particularly to FIGURE 1, there is shown receiver 10 which utilizes antenna 12 feeding into preamp assembly 14. Antenna preamp assembly 14 feeds into L1/L2 frequency selector 16 which sends signals to L-band down conversion 18. These components all operate under the control of reference oscillator 20 and frequency synthesizer 22. Reference oscillator 20 and frequency synthesizer 22 provide oscillation for L-band down conversion 18. Output from L-band down conversion 18 is a second IF that goes into an analog-to-digital converter (A/D)

with automatic gain control (AGC) circuit 24. The output of this A/D circuit is then channelized to code and carrier wipe off in circuits 26, 28 and 30. This is where the remote signal transmitted by the GPS satellite is compared and matched with the receiver's estimate of the remote signal.

The outputs of signal processing circuits, 26, 28 and 30 are shown as signals 32 into processor computer 34. Processor computer 34 provides signals 36 to signal processing circuit 26, 28 and 30 to direct the circuits to change their code and carrier estimates, as well as for general control of the circuits.

Each signal processing circuit 26, 28 and 30, uniquely and completely generates carrier estimates, code estimates, base band pre-detection estimates and contains all the correlators for signal processing as well as provides autonomous signal search capability for two satellites. Each channel also has the capability to simultaneously track both the C/A-code and P-code. whereever used herein the term P-code shall include P(Y)-code.

FIGURE 2 shows how a typical method to perform pre-detection integration in single C/A- and P-code channel 37. This channel 20 can only track L1 C/A- and P-code or L2 P-code. Carrier generator 36 generates a complex estimate of the incoming GPS carrier. Carrier mixer 38 wipes off the incoming carrier. P-code clock generator 40 and P-code generator 42 generate an estimate of P-code and C/A- code clock generator 44 and C/A-code generator 46 generate an estimate of the C/A-code. P-code delay shift register 48 and C/A-code delay shift register 50 generate a plurality of P-code and C/A-code phases 1/2-chip apart, respectively. Finally, code is wiped off in P-code mixers 52 and C/A-code mixers 54. Pre-detection integration is then performed using an integrate circuit 56.

Six correlators are shown so the P-code and C/A-code can be track simultaneously (three for P-code and three for C/A-code). In addition, it is possible to dedicate all six correlators to C/A-code using correlator switches 58 for search modes of operation. This is done so that C/A-code can be found more quickly in typical search operations.

For some applications of GPS, it is desirable to be able to track L1 and L2 simultaneously. Hardware aside, the easiest way to do this is with an independent tracking loop for L1 and L2. By enhancing the previously described channel 37, it is possible to get the benefit of independent L1 and L2 tracking without the penalty of having two independent channels. For some operational scenarios, it also may be desirable to be able to switch between having two independent tracking loops and having one tracking loop with a phase delta between L1 and L2. Two independent loops would be used in hostile environments where there is a good possibility of losing either L1 or L2. One tracking loop may be desirable for less processor throughout when there is no threat of losing the main L-band. Within a P-code receiver such as that of FIGURE 1, the present invention allows this operational flexibility. For these purposes, FIGURE 3 describes an enhanced single P-code L1/L2 channel that may be used to enhance the capability of signal processing circuits 26, 28 and 30.

FIGURE 3 shows an enhanced L1/L2 channel 60 according to the present invention. The modified P-code clock generator 62 generates two P-code clocks with same frequency and independent phase, one for L1 and one for L2. The modified P-code clock generator 62 also detects which of these clock lead. The leading clock is used to clock P-code generator 64. Each new P-code chip is stored in the next location of the P-code circular buffer 302. P-code clock generator 62 is used to increment the L1 and L2 P-code chip counters 68 and 70, respectively. Whenever the L1 P-code chip counter, 68, is incremented, 16-to-1 MUX 70 passes the next P-code chip stored in the P-code circular buffer 66 to the L1 P-code delay shift register 76. The L2 P-code chip counter 72 and 16-to-1 MUX 74 are implemented and work in exactly the same manner as the L1 P-code chip counter 68 and 16-to-1 MUX, 70. Thus, from one P-code generator 64 two P-code outputs, one for L1 and one for L2, go to code delay shift registers, 76 and 78, respectively. This represents a considerable savings in circuitry because P-code generator 64 comprises numerous gates and additionally requires significant computer processing capability to support its operation. Although the preferred embodiment requires a separate carrier generator for each signal frequency, carrier generators for L1 and L2 are easy to build and do not consume nearly as much power as would a second complete channel.

The enhanced L1/L2 channel 60 of FIGURE 3 provides maximum operational flexibility with minimal additional circuitry. Circuits which are not changed from the previously described typical C/A- and P-code channel include the P-code generator 64, C/A-code clock generator 44, and C/A-code generator 46. The carrier generators, 80 and 82, and carrier mixers, 84 and 86 are the same as the previously shown carrier generator 36 and carrier mixer 38, except that L1 carrier generator 80 is always configured to generate an L1 carrier and the L2 carrier generator 82 is always configured to generate an L2 carrier. Also, the code delay shift registers, 76,78 and 88, code mixers, 90, 92 and 94, the pre-detection integration circuitry 96, and correlator switches 98 and 100 are implemented and function such as the code delay shift registers 48 and 50, coder mixers, 52 and 54, the pre-detection integration circuitry 56 and the correlator switches 58 shown in the typical C/A- and P-code channel 37 of FIGURE 2. The only difference being that there is an extra set of P-code delay shift registers 78, P-code mixers 92 and correlator switches 100 and that the

pre-detection integration circuitry 332 supports three additional correlators. This is done to accommodate the extra three correlators required to track L2 P-code.

Unique to the enhanced channel is a modified P-code clock generator 62, a P-code circular buffer 66, two P-code chip counters, 68 and 72, and two 16-to-1 multiplexers (MUX), 70 and 74.

FIGURE 4 shows a high level block diagram of the modified P-code clock generator 62. This circuit is a unique modification of the low-powered digital oscillator detailed in co-pending application entitled "Method and Systems for a Multi-Channel Global Position System Signal Processor". Circuitry to determine which clock leads is not shown. One approach to determine the leading clock is to extend the P-code chip counters 68 and 74 an extra two bits and compare the counter values to see which clock leads.

The circuit operation of the modified P-code clock generator 62, is basically the same as the code clock generator described in the previously mentioned co-pending U.S. Patent Applications. The modification is that there are two separate 16-bit P-code clock phase words 112 and 114, one for determining the phase of the L1 P-code clock and the other for determining the phase of the L2 P-code clock. Since initial P-code clock phase only affects the 13 most significant bits of the 32-bit P-code clock generator adder/accumulator, the 19 least significant bits of the adder/accumulator 122 are common to both the L1 and the L2 P-code clock. The frequency word 116 is also common to both the L1 and L2 P-code clock. Along with the two separate P-code clock phase words, 112 and 114 are two 13-bit adder/accumulators 118 and 120 one for L1 P-code clock and one for L2 P-code clock, which together with the 19-bit adder/accumulator 122 make up two separate 32-bit adder/accumulators capable of generating carriers to the two state machines 124 and 126 with the same frequency but different phase. The state machine and carry delay circuits 124 and 126 are exactly the same as described in the previously mentioned co-pending U.S. Patent Applications.

FIGURE 5 shows the estimated difference between a typical single L-band channel and the enhanced L1/L2 channel of the present invention. An enhanced channel requires only 42% additional circuitry over a normal channel and provides the performance benefit and software reduction of two completely independent channels for tracking L1 and L2 simultaneously.

The cost of the enhanced channel is considerably less than the 42% when overhead circuitry such as channel timing and control, processor interface and search specific circuits are included in the gate count estimates. Also note that for this specific example, that the enhanced channel has three additional correlators. This provides approximately a 50% improvement in search speed. As a result of the enhanced P-code channel of the present invention, there is provided an apparatus and method for significantly increasing GPS system receiver channel flexibility without a significant increase in circuitry or software complexity.

Although this description describes the invention with reference to the above specific embodiments, the claims, and not this description, limit the scope of the invention. Various modifications or the disclosed embodiment, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the above description. Therefore, the appended claims will cover such modification that follow up in the true scope of the invention.

Aspects of the present invention will be further appreciated from the following:

The P-Code Channel on-a-chip (PCOAC) to be described is a dual channel GPS signal processor integrated circuit. A 95-pin ceramic pin-grid-array (PGA) contains the 348,300 transistor CMOS gate array. Major features include: two independent GPS channels; a search processor for improved acquisition time; an embedded Y-code generator; system synchronization control; and a 16-bit processor interface.

Figure 16 shows a block diagram of PCOAC 1010. Unused functions can be turned off allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Each channel of circuit 1010 is a dedicated signal processing circuit which de-modulates the code and carrier of a GPS signal and performs pre-detection integration. Each channel contains a code clock generator 1103 (1104), a P and C/A-code generator 1105 (1106), an L1/L2 carrier generator 1109 (1110), eight correlators 1111, 1113, 1115, 1117 (1112, 1114, 1116, 1118) and a noise meter 1119 (1120). Each of the eight correlators can be selected to operate with C/A-code or P-Code. A Y-code generator 1108 common to both channels provides independent Y-code for both channels.

Search processor 1123 and discrete fourier transform (DFT) function 1124 improve signal acquisition capability. The DFT separates the sample integration data into seven frequency bins. Search processor 1123 interpolates between these seven frequency bins to obtain six additional frequency bins, producing a total of thirteen frequency bins per correlator. The search processor implements a Tong detection algorithm on all eight correlators for each of the thirteen frequency bins resulting in the simultaneous search of 1104 search bins per channel.

PCOAC 1010 supports three frequency plans, 57.7920 MHz, 40.9216 MHz and 40.9200 MHz operation. Several programmable clocks/interrupts 1130 are provided to synchronize the host processor to

PCOAC operation. Various interrupt schemes are designed to allow trade-offs to be made between system performance, processor throughput requirements and the complexity of the software.

A standard 16-bit processor interface 1131 is utilized. In order to minimize read/write overhead to the PCOAC, integration samples are buffered 1121 (1122) and the memory map is designed so that block moves are all that is required for channel updates during normal tracking operations.

Figure 7 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC 10: Base Band Module 1130 generates several global clocks for system synchronization;

Channel Timing Module 1101 generates all clocks and synchronization pulses specific to a single channel;

Code Generator Module 21 includes a programmable code clock generator, P-code and C/A-code generators/setters, and P-code and C/A-code state advance and retard for search;

Y-Code Generator Module 1108 converts the P-code into Y-code for both channels simultaneously even during code state advances;

Front-End Correlator Module 1201 provides L1 or L2 carrier generation, a carrier mixer, a P-code and C/A-code delay shift register (to generate eight code phases), code mixers, data wipe-off, and noise meter signal selection;

Intermediate Correlator Module 1202 performs the first stage of sample integration for eight complex correlators and a noise meter;

Black-End Correlator Module 1203 performs the final stage of sample integration, and also performs noise measurement for aiding in search and tracking (one per channel);

IRAM 1204 and Q RAM 1205 are two 64 x 16-bit 3-port RAMs per channel for sample integration buffering or to hold intermediate values for DFT calculations;

Discrete Fourier Transfor (DFT) Module 1124 converts integration samples from all correlators of both channels into seven frequency bins of sample data for search operations;

Search Processor Module 1206 interpolates six additional frequency bins from those provided by the DFT module, performs Tong detection on all thirteen frequency bins of data and retards the code state until a signal is found;

Search Processor RAM 1207 is a 64 x 16-bit 3-port RAM used by the search processor as a holding register for active Tong counts during search or noise measurement buffering during tracking;

Processor Interface Module 1131 provides address decode to generate internal read and write strobes, integration sample buffering control, a programmable ring oscillator for test and other miscellaneous functions.

Digital signal processing circuitry as exemplified herein may be implemented by means of a single integrated circuit.

Claims

1. An enhanced P-code channel for use in a GPS receiver, said channel being adapted for simultaneously tracking L1 and L2 and comprising:
a P-code clock generator for generating two code clocks, the first clocks associated with L1 and the second of said code clocks associated with L2, said code clocks having the same frequency but different phase from one another;
circuitry for generating a plurality of P-code chips and storing a plurality of the most recently generated of said P-code chips;
a first circuit for selecting and update P-code chips from said stored plurality of P-code chips said selected and updated chips being in phase with said L-1 code clock;
a second circuit for selecting and updating P-code chips from said stored plurality of P-code chips said selected and updated chips being in phase with said L-2 code clock.

2. A multi-channel GPS signal processor for use in a GPS receiver, said processor comprising:
digital signal processing circuitry on a single integrated circuit for acquiring and tracking valid P-code signals from at least one satellite of said GPS system; and
an enhanced P-code channel as claimed in claim 1.

3. A receiver for determining geographical position, velocity, and time from analog signal information received from a plurality of navigational satellites, said signal information having data shifts dependent upon distance and frequency shifts dependent upon the relevant velocity between the satellite's transmission position and the geographical position of said receiver, wherein said analog signal is significantly weaker than ambient atmospheric noise, said receiver comprising:
a digital signal processing circuit for acquiring said signal in the presence of said noise, for estimating the current position and for correcting said estimate based upon data exchanged between said digital signal processing circuit and said processor;
an enhanced P-code channel associated within said digital processing circuit for use in said receiver, said channel capable of simultaneously tracking L1 and L2 and comprising:
a single P-code clock generator for generating two code clocks, a first of said code clocks asso-

ciated with L1 and a second of said code clocks associated with L2, said code clocks having the same frequency but different phase from each other;

circuitry for generating a plurality of P-code chips and storing a plurality of said P-code chips, said P-code chips being those most recently generated by said digital signal processing circuit;

a first circuit for selecting and updating P-code chips from said plurality of chips, said chips being in phase with said L1 code clock; and

a second circuit for selecting and updating P-code chips from said stored plurality of chips, said chips being in phase with said L2 code clock.

4. The apparatus of any of Claims 1-3, further comprising a P-code circular buffer within said generating and storing circuitry for generating two phases of P-code for tracking L1 and L2.

5. The apparatus of Claim 4, wherein said channel is associated to independently track L1 or L2.

6. The apparatus of any of Claims 1-3, further comprising circuitry for simultaneously generating C/A-code for L1, P-code for L1, and P-code for L2.

7. The apparatus of Claim 6, further comprising circuitry for vector summing said C/A-code for L1, P-code for L1, and P-code for L2, thereby increasing sensitivity of said channel.

8. The apparatus of any of Claim 1-3, further comprising circuitry for continuous ionospheric correction within said channel.

9. A method for simultaneously tracking L1 and L2 in a single P-code channel for use in the GPS receiver, said method comprising the steps of:

generating two code clocks using a single P-code clock generator, the first of said code clocks being associated with L1 and the second of said code clocks being associated with L2, said code clocks further having the same frequency but different phases;

generating a plurality of P-code chips;

storing a plurality of the most recently generated of said P-code chips;

selecting and updating P-code chip addresses from said stored plurality of P-code chips in phase with said L1 code clock; and

selecting and updating P-code chips from said stored plurality of chips in phase with said L2 code clock.

10. The method of Claim 9, further comprising the step of tracking L1 in said channel for assisting L2 tracking.

11. The method of Claim 9, further comprising the step of tracking L2 in said channel to a tracking of L1.

12. A method for determining geographical position, velocity, and time from analog signal information received from a plurality of navigational satellites, said signal information having data shifts depending upon distance and frequency shifts depended upon the relative velocity between the satellite's transmission position and the geographical position of said receiver, wherein said analog signal is significantly weaker than ambient atmospheric noise, said method comprising the steps of:

acquiring said signal in the presence of said noise, estimating the current position, and correcting said estimate; and

simultaneously tracking L1 and L2 in a single enhanced P-code channel said tracking step comprising the steps of:

generating two code clocks using a single P-code clock generator the first of said code clocks being associated with L1 and the second of said code clocks associated with L2, said code clocks further having the same frequency but different phases;

generating a plurality of P-code chips;

storing a plurality of the most recently generated of said P-code chips;

selecting and updating P-code chip addresses from said stored plurality of P-code chips in phase with said L1 code clock; and

selecting and updating P-code chips from said stored plurality of chips in phase with said L2 code clock.

13. The method of Claim 12, further comprising the step of generating two phases of P-code for tracking L1 and L2 separately.

14. The method of either of Claims 9 or 12, further comprising the step of independently tracking L1 or L2.

15. The method of either Claims 9 or 12, further comprising the step of simultaneously generating C/A-code for L1, P-code for L1, and P-code within said single enhanced channel.

16. The method of Claim 15, further comprising the step of vector summing said C/A-code for L1, P-code for L1 and P-code for L2.

17. The method of either of Claims 9 or 12, further

comprising the step of continuously performing ionospheric correction within said channel.

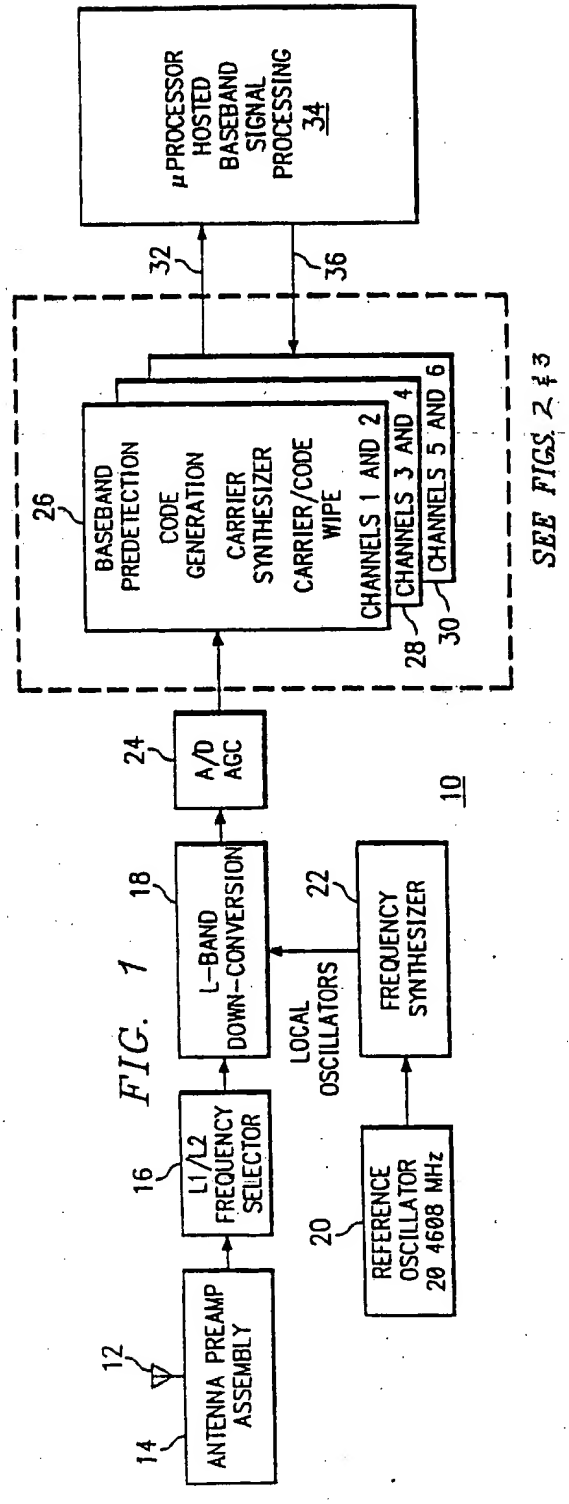


FIG. 1

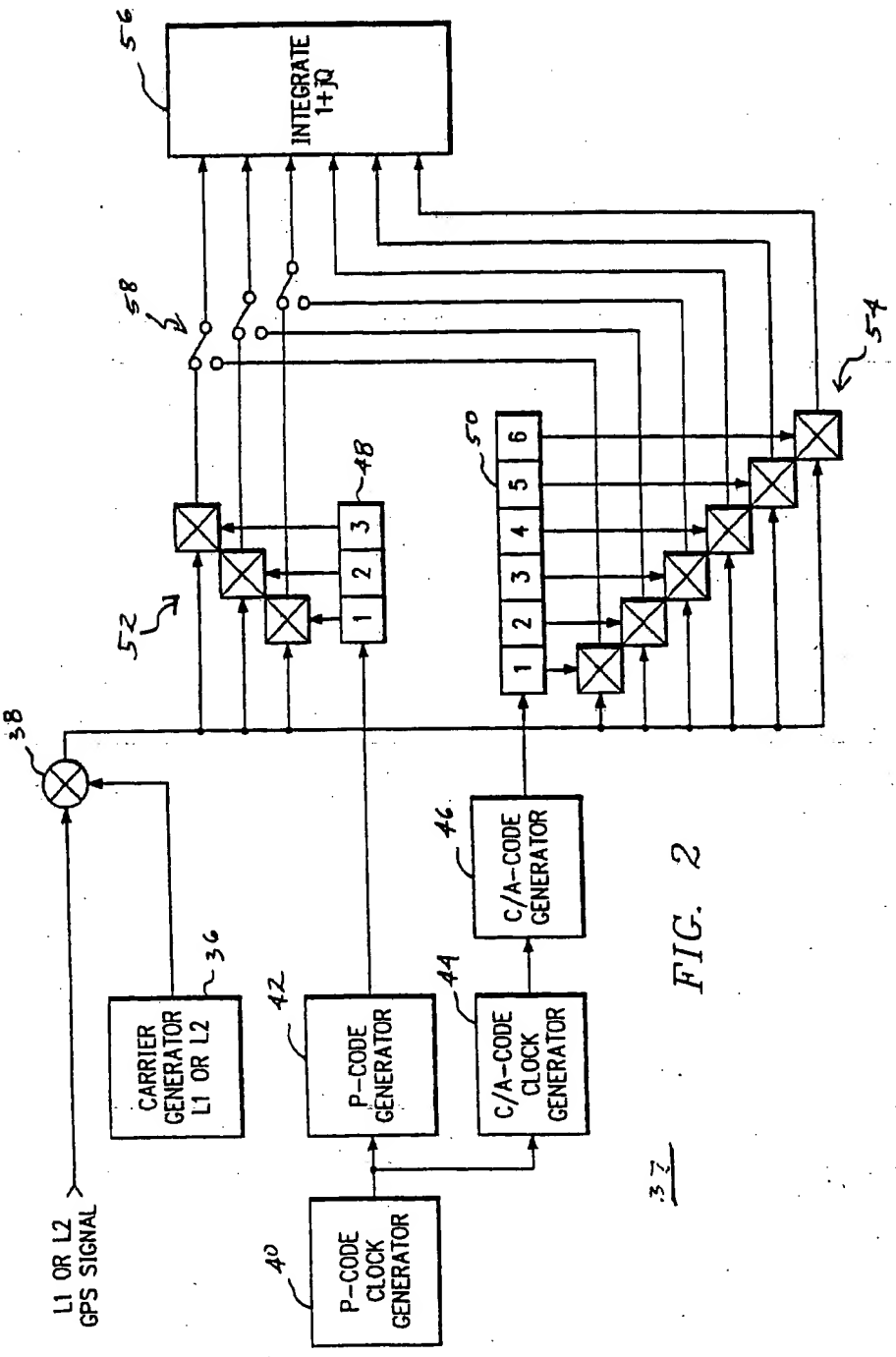


FIG. 2

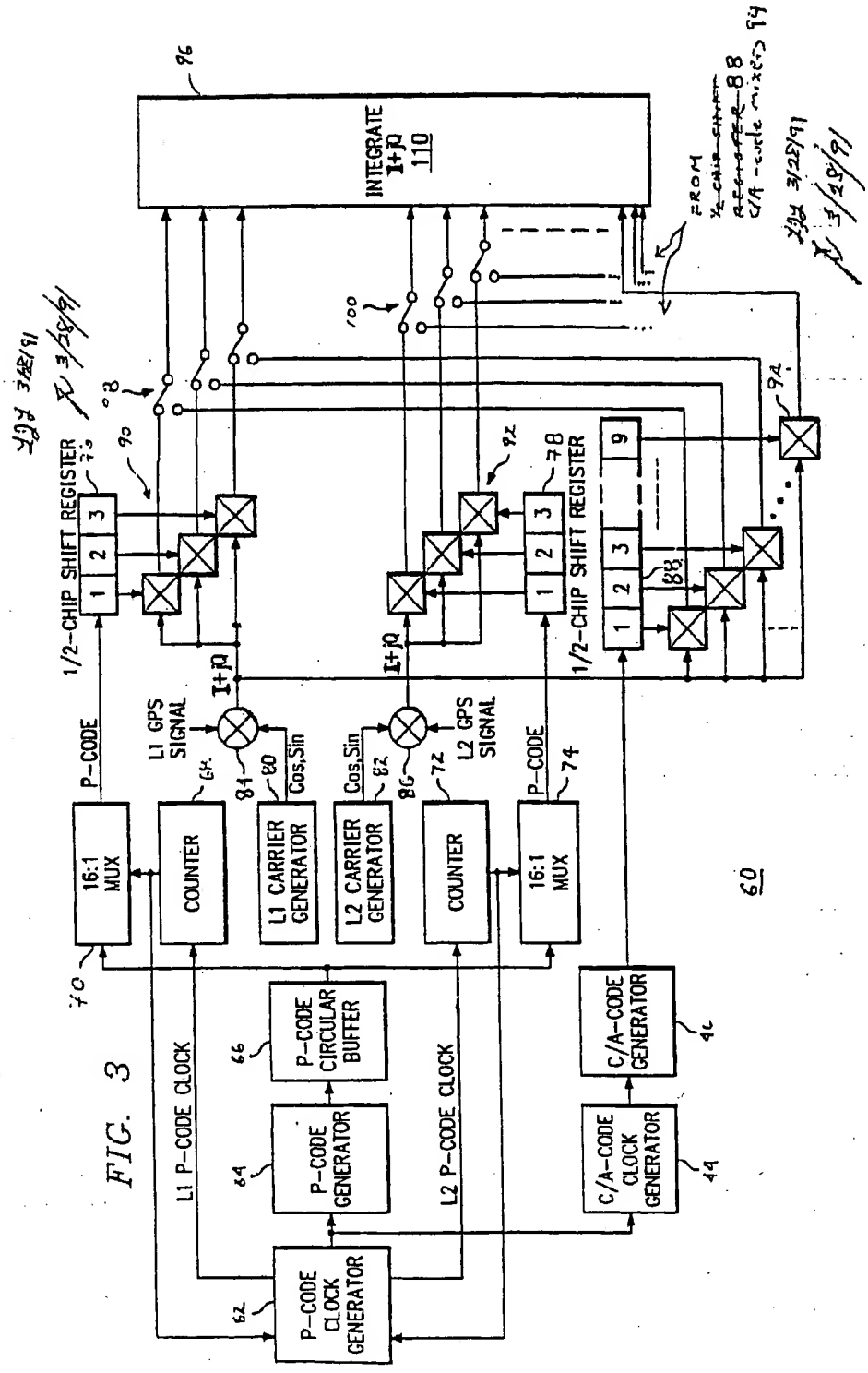


FIG. 3

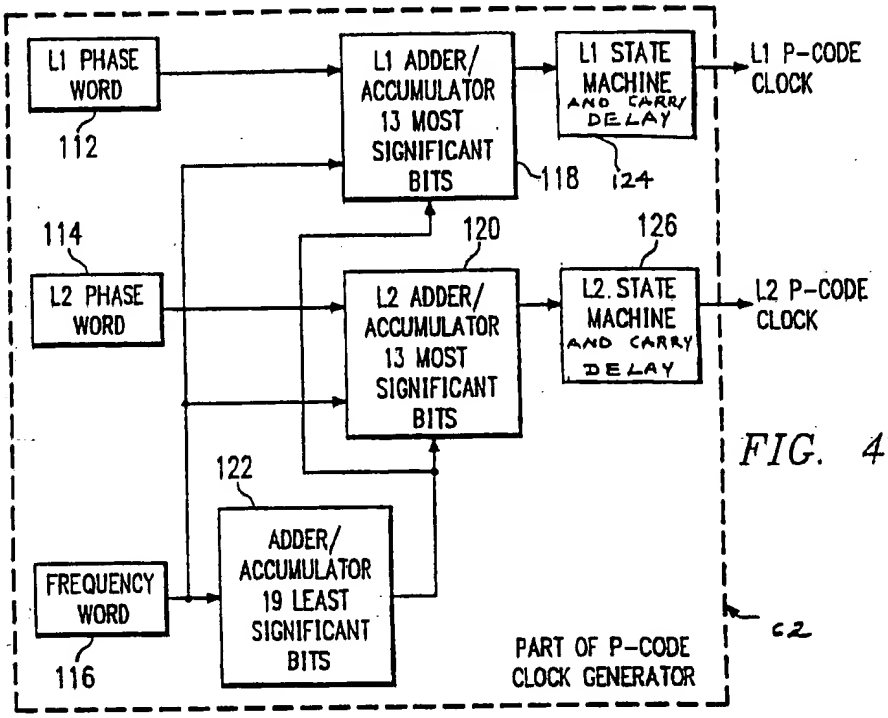
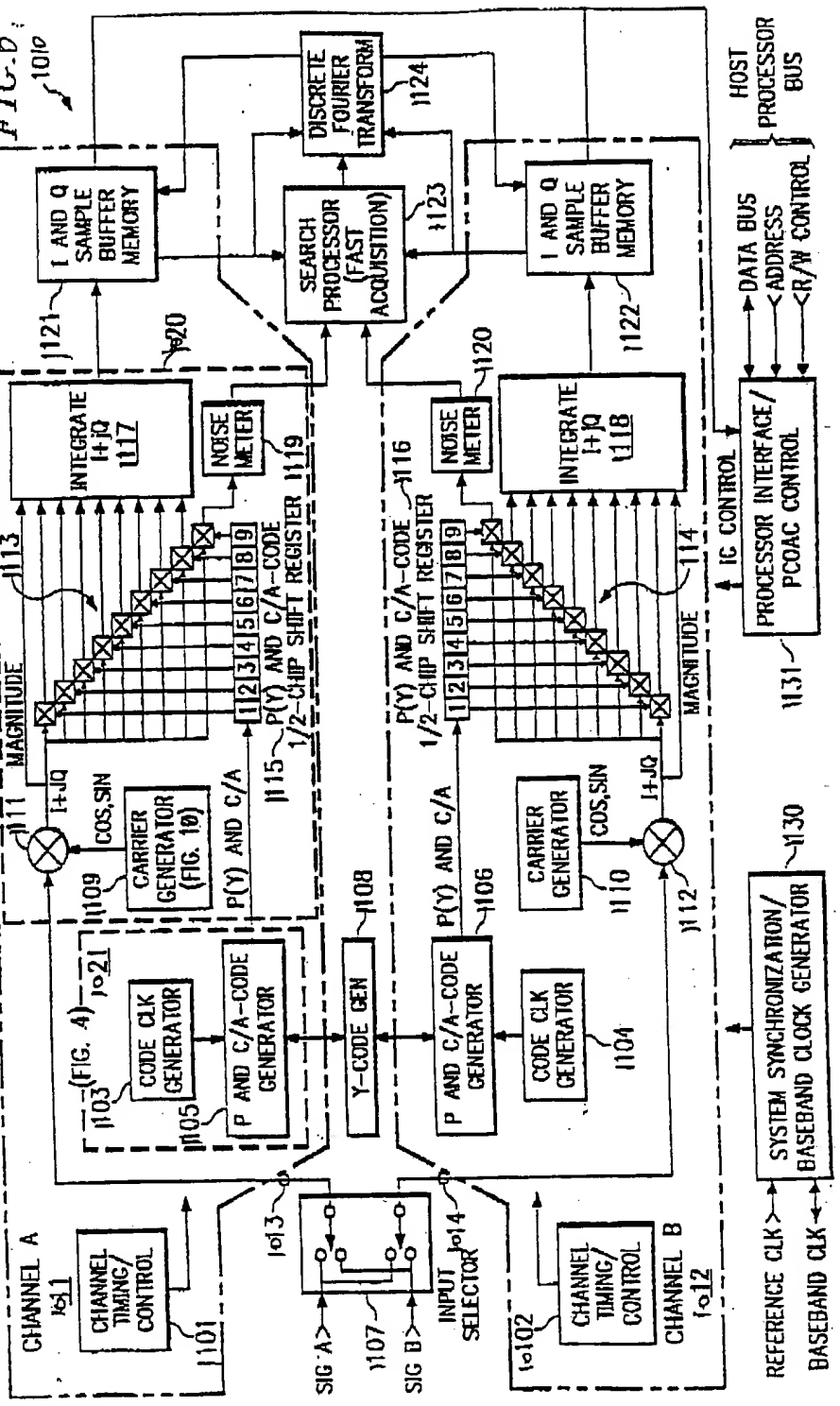


FIG. 4

FIG. 5 GATE COUNT OF PRIOR ART CHANNEL VERSUS ENHANCED L1/L2 CHANNEL

FUNCTION	TYPICAL		ENHANCED	
	QTY	GATES	QTY	GATES
CARRIER GENERATOR 36, 80, 82	1	1244	2	2488
CARRIER MIXER 38, 84, 86	1	126	2	252
P-CODE CLOCK GEN. 40, 62	1	1246	1.5	1869
P-CODE GENERATOR 42, 64	1	3000	1	3000
CIRCULAR BUFFER 66	0	0	1	150
COUNTER 68, 72	0	0	2	60
16:1 MULTIPLEXER 70, 74	0	0	2	66
P-CODE DELAY SHIFT REG. 48, 76, 78	1	25	2	50
P-CODE MIXERS 52, 90, 92	3	9	6	18
C/A-CODE CLOCK GEN. 44	1	50	1	50
C/A-CODE GEN. 46	1	500	1	500
C/A-CODE DELAY SHIFT REG. 50, 88	1	50	1	75
C/A-CODE MIXERS 54, 94	6	18	9	27
CORRELATOR SWITCH 58, 98, 100	3	9	6	18
INTEGRATORS 56, 96	6	4100	9	6150
TOTAL	10,377		14,773	

FIG. 6



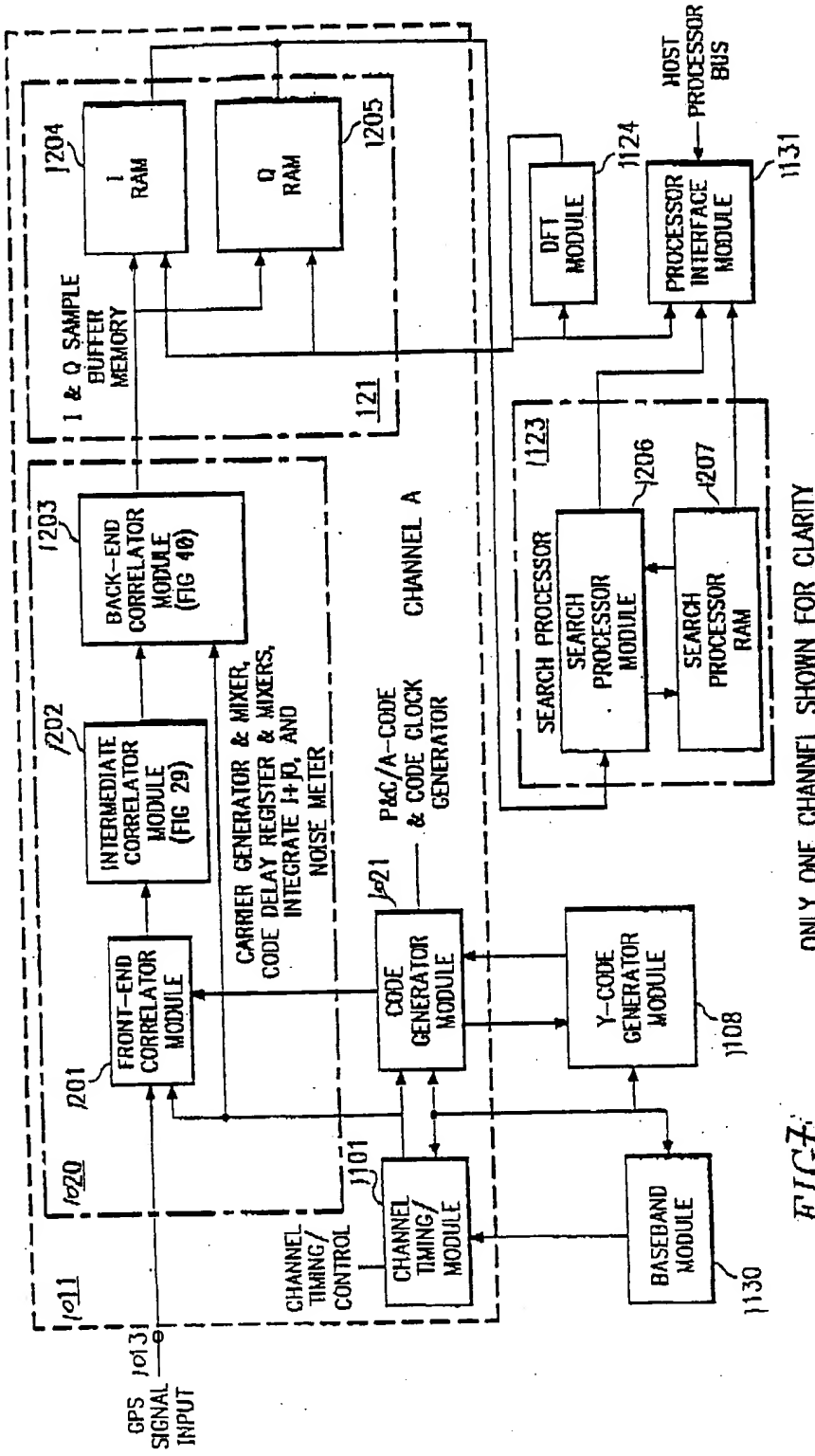


FIG 7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 92302791.6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	US - A - 4 035 663 (ROCKWELL)	1-3,9, 12	G 01 S 5/08 G 01 S 11/08
A	* Abstract; claims *	4-8, 10,11, 13-17	
Y	US - A - 4 613 977 (STC)	1-3,9, 12	
A	* Abstract; claims *	4-8, 10,11, 13-17	
A	US - A - 4 189 622 (NCR) * Abstract; claims *	1-17	
A	US - A - 4 468 793 (TI) * Abstract; claims *	1-17	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 01 S 5/00
G 01 S 11/00
H 03 K 19/00
H 04 B 1/00
H 04 L 7/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	25-05-1992	BLASL

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)